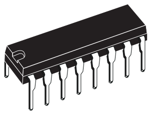
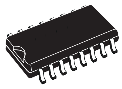
# STP08CDC596

## 8-BIT CONSTANT CURRENT LED SINK DRIVER WITH FULL OUTPUT DETECTION

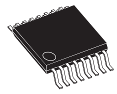
- 8 CONSTANT CURRENT OUTPUT CHANNELS
- ADJUSTABLE OUTPUT CURRENT THROUGH ONE EXTERNAL RESISTOR
- OPEN AND SHORT LINE, SHORT TO GND, SHORT TO V-LED SUPPLY ERROR DETECTION
- SERIAL DATA IN/PARALLEL DATA OUT
- SERIAL OUT CHANGE STATE ON THE FALLING EDGES OF CLOCK
- OUTPUT CURRENT: 20-120 mA
- 25 MHz CLOCK FREQ.



DIP-16



SO-16



TSSOP16

### DESCRIPTION

The STP08CDC596 is a monolithic, medium-voltage, low current power 8-bit shift register designed for LED panel display. The STP08CDC596 contains a 8-bit serial-in, parallel-out shift register that feeds a 8-bitD-type storage register. In the output stage, eight regulated current sources were designed to provide 15-120mA constant current to drive the LEDs.
The STP08CDC596 contains the built-IN error detection feature. The device performs this additional function without any increase of the pin number and any change of the pin function, if compared to the standard device without error detection. Consequently, choosing this device does not mean to change the footprint on the board. To perform this functionality mode, the device needs a digital key coming from the Microprocessor. The STP08CDC596 is able to detect: open and short on the LED line, short to GND, short to Led voltage supply. The data mapping of output channels status detection is provided by a feedback from the serial output to the Microprocessor.
Trough an external resistor, users may adjust the STP08CDC596 output current, controlling the light intensity of LEDs.
The STP08CDC596 guarantees 16V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 25 MHz, also satisfies the system requirement of high volume data transmission.
The device is offered in DIP-16, SO-16 and TSSOP-16 packages.
The STP08CDC596 is well suitable for traffic display signs where the detection feature is strongly required.

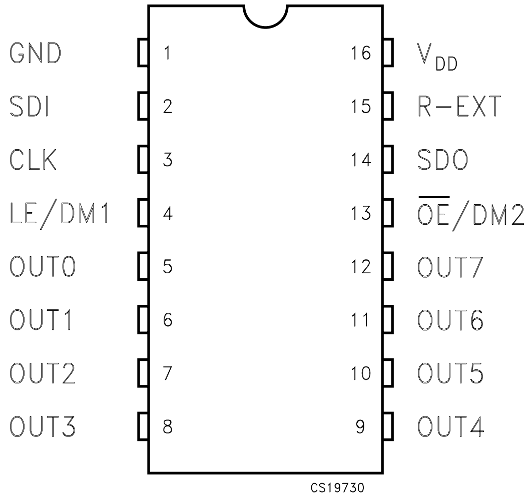
**Table 1: Order Codes**

| Type | Temp. Range | Package | Comments |
|---|---|---|---|
| STP08CDC596B1 | -40°C to 125°C | DIP-16 | 25 part per tube |
| STP08CDC596M | -40°C to 125°C | SO-16 (Tube) | 50 parts per tube |
| STP08CDC596MTR | -40°C to 125°C | SO-16 (Tape & Reel) | 2500 parts per reel |
| STP08CDC596TTR | -40°C to 125°C | TSSOP16 (Tape & Reel) | 2500 parts per reel |

### Table 2: Current Accuracy

| Output Voltage | Current accuracy | | Output Current |
|---|---|---|---|
| | Between bits | Between ICs | |
| ≥ 0.7V | TYP. ± 3% | ± 10% | 20 to 120 mA |

### Figure 1: Pin Connection




### Table 3: Pin Description

| PIN N° | Symbol | Name and Function |
|---|---|---|
| 1 | GND | Ground Terminal |
| 2 | SDI | Serial data input terminal |
| 3 | CLK | Clock input terminal |
| 4 | LE/DM1 | Latch input terminal |
| 5-12 | OUT 0-7 | Output terminal |
| 13 | $\overline{OE}$/DM2 | Output enable input terminal (active low) |
| 14 | SDO | Serial data out terminal |
| 15 | R-EXT | Constant Current programming |
| 16 | $V_{DD}$ | 5V Supply voltage terminal |

### Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 0 to 7 | V |
| $V_O$ | Output Voltage | -0.5 to 16 | V |
| $I_O$ | Output Current | 120 | mA |
| $V_I$ | Input Voltage | -0.4 to $V_{DD}$+0.4 | V |
| $I_{GND}$ | GND Terminal Current | 980 | mA |
| $f_{CLK}$ | Clock Frequency | 25 | MHz |
| $T_{OPR}$ | Operating Temperature Range | -40 to +125 | °C |
| $T_{STG}$ | Storage Temperature Range | -55 to +150 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

**Table 5: Thermal Data**

| Symbol | Parameter | DIP-16 | SO-16 | TSSOP16 | Unit |
|---|---|---|---|---|---|
| $R_{thj-amb}$ | Thermal Resistance Junction-ambient | 90 | 125 | 140 | °C/W |

**Table 6: Recommended Operating Conditions**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 3.3 | | 5.5 | V |
| $V_O$ | Output Voltage | | | | 16.0 | V |
| $I_O$ | Output Current | OUTn | 15 | | 120 | mA |
| $I_{OH}$ | Output Current | SERIAL-OUT | | | +1 | mA |
| $I_{OL}$ | Output Current | SERIAL-OUT | | | -1 | mA |
| $V_{IH}$ | Input Voltage | | $0.7V_{DD}$ | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input Voltage | | -0.3 | | $0.3V_{DD}$ | V |
| $t_{wLAT}$ | LE/DM1 Pulse Width | $V_{DD}$ = 3.0 to 3.6V | | 10 | 20 | ns |
| $t_{wCLK}$ | CLK Pulse Width | | | 10 | 20 | ns |
| $t_{wEN}$ | $\overline{OE}$/DM2 Pulse Width (1) | | | 120 | 400 | ns |
| $t_{SETUP(D)}$ | Setup Time for DATA | | | 5 | 20 | ns |
| $t_{HOLD(D)}$ | Hold Time for DATA | | | 4 | 15 | ns |
| $t_{SETUP(L)}$ | Setup Time for LATCH | | | 8 | 15 | ns |
| $f_{CLK}$ | Clock Frequency (2) | | | | 25 | MHz |

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.
(2) In normal mode the $\overline{OE}$/DM2 must remain low at least two clock cycles.

**Table 7: Electrical Characteristics** ($V_{DD}$=5V, T = 25°C, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input Voltage High Level | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{IL}$ | Input Voltage Low Level | | GND | | $0.3V_{DD}$ | V |
| $I_{OH}$ | Output Leakage Current | $V_{OH}$ = 16 V | | | 10 | μA |
| $V_{OL}$ | Output Voltage (Serial-OUT) | $I_{OL}$ = 1mA | | | 0.4 | V |
| $V_{OH}$ | Output Voltage (Serial-OUT) | $I_{OH}$ = -1mA | $V_{DD}$-0.4V | | | V |
| $I_{OL1}$ | Output Current | $V_O$ = 0.7V $R_{EXT}$ = 910 Ω | 18.8 | 20.9 | 24.00 | mA |
| $I_{OL2}$ | | $V_O$ = 0.7V $R_{EXT}$ = 360 Ω | 46.00 | 51.5 | 56.5 | mA |
| $\Delta I_{OL1}$ | Output Current Error between bit (All Output ON) | $V_O$ = 0.7V $R_{EXT}$ = 910 Ω | | ± 2 | ± 5 | % |
| $\Delta I_{OL2}$ | | $V_O$ = 0.7V $R_{EXT}$ = 360 Ω | | ± 1 | ± 4 | % |
| $R_{SIN(up)}$ | Pull-up Resistor | | 150 | 300 | 600 | KΩ |
| $R_{SIN(down)}$ | Pull-down Resistor | | 100 | 200 | 400 | KΩ |
| $I_{DD(OFF1)}$ | Supply Current (OFF) | $R_{EXT}$ = OPEN OUT 0 to 7 = OFF | | 0.45 | 0.7 | mA |
| $I_{DD(OFF2)}$ | | $R_{EXT}$ = 910 Ω OUT 0 to 7 = OFF | | 3.0 | 6.0 | |
| $I_{DD(OFF3)}$ | | $R_{EXT}$ = 360 Ω OUT 0 to 7 = OFF | | 8.2 | 12.0 | |
| $I_{DD(ON1)}$ | Supply Current (ON) | $R_{EXT}$ = 910 Ω OUT 0 to 7 = ON | | 3.1 | 6.2 | |
| $I_{DD(ON2)}$ | | $R_{EXT}$ = 360 Ω OUT 0 to 7 = ON | | 8.4 | 12.8 | |

**Table 8: Switching Characteristics** ($V_{DD}$=3.3 to 5.5V, T = 25°C, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH1}$ | Propagation Delay Time, CLK-OUTn, LE/DM1 = H, OE/DM2 = L | $V_{DD}$ = 3 V, $V_{IH}$ = $V_{DD}$, $V_{IL}$ = GND, $C_L$ = 13pF, $I_O$ = 40mA, $V_L$ = 3 V, $R_{EXT}$ = 470 Ω, $R_L$ = 65 Ω | | 180 | 280 | ns |
| $t_{PLH2}$ | Propagation Delay Time, LE/DM1-OUTn, OE/DM2 = L | | | 150 | 280 | ns |
| $t_{PLH3}$ | Propagation Delay Time, OE/DM2-OUTn, LE/DM1 = H | | | 140 | 280 | ns |
| $t_{PLH}$ | Propagation Delay Time, CLK-SDO | | | 25 | 35 | ns |
| $t_{PHL1}$ | Propagation Delay Time, CLK-OUTn, LE/DM1 = H, OE/DM2 = L | | | 30 | 60 | ns |
| $t_{PHL2}$ | Propagation Delay Time, LE/DM1-OUTn, OE/DM2 = L | | | 30 | 50 | ns |
| $t_{PHL3}$ | Propagation Delay Time, OE/DM2-OUTn, LE/DM1 = H | | | 35 | 70 | ns |
| $t_{PHL}$ | Propagation Delay Time, CLK-SDO | | | 30 | 40 | ns |
| $t_r$ | Output Rise Time | | | 220 | | ns |
| $t_f$ | Output Fall Time | | | 20 | | ns |

## EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

**Figure 2: $\overline{OE}$/DM2 Terminal**

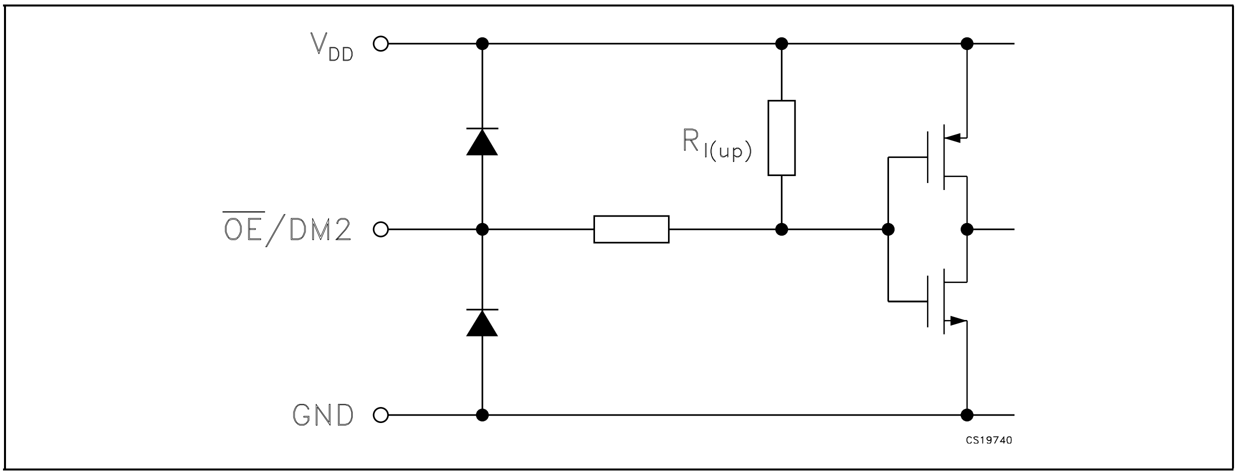


**Figure 3: LE/DM1 Terminal**

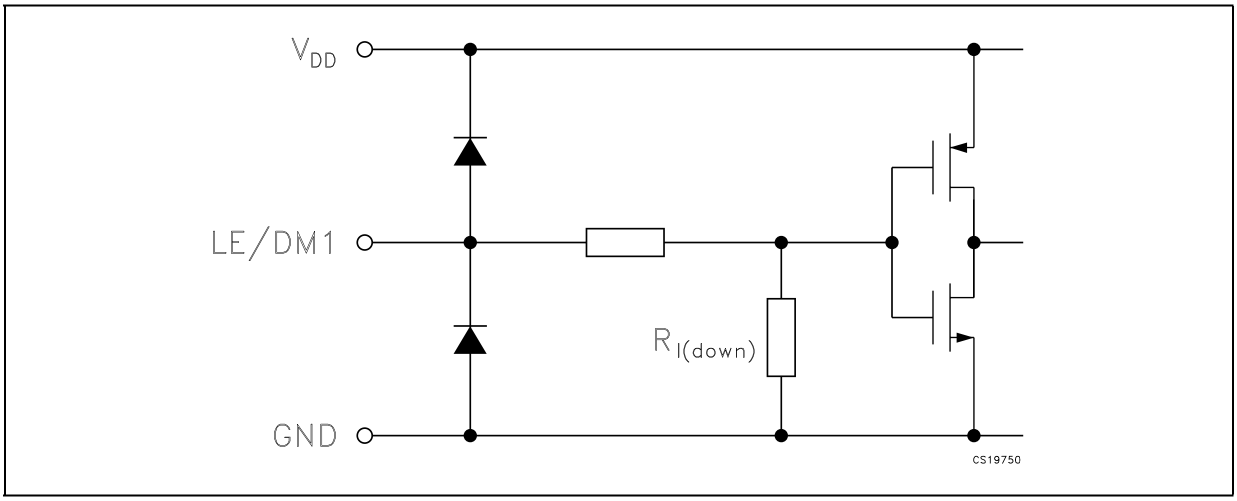



**Figure 4: CLK, SDI Terminal**

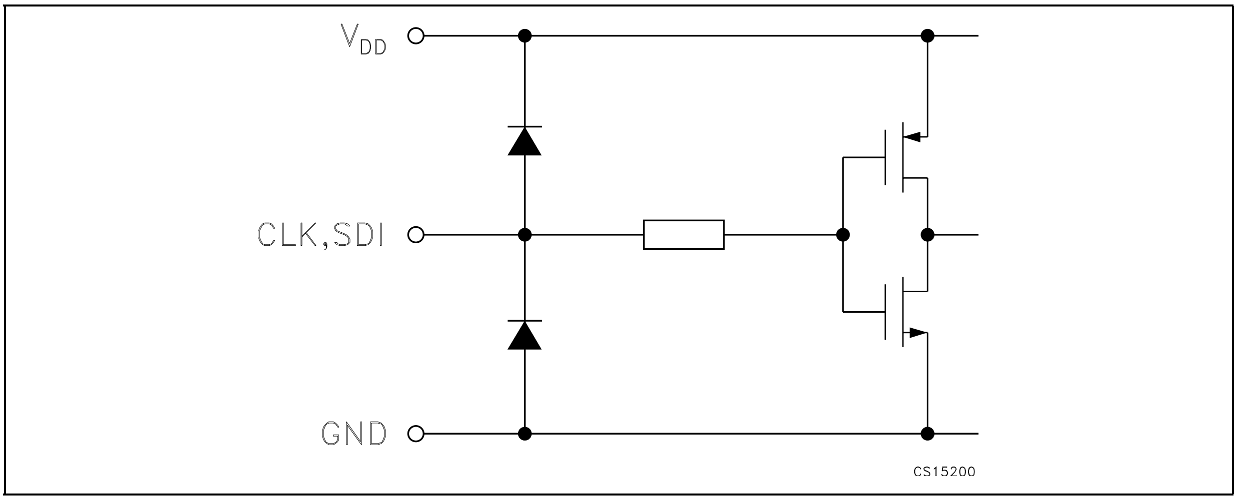



**Figure 5: SDO Terminal**

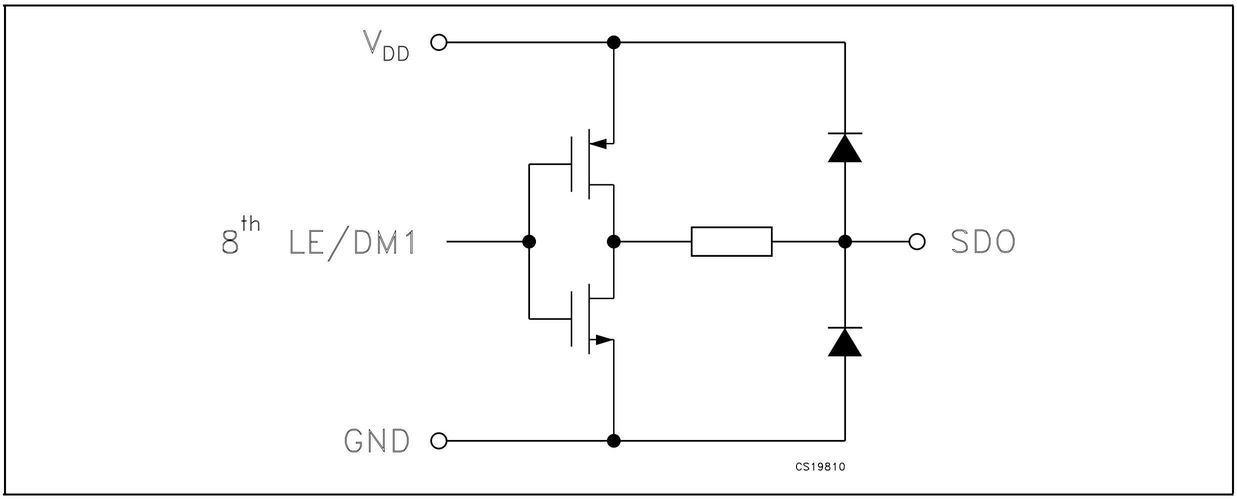


**Figure 6: Block Diagram**

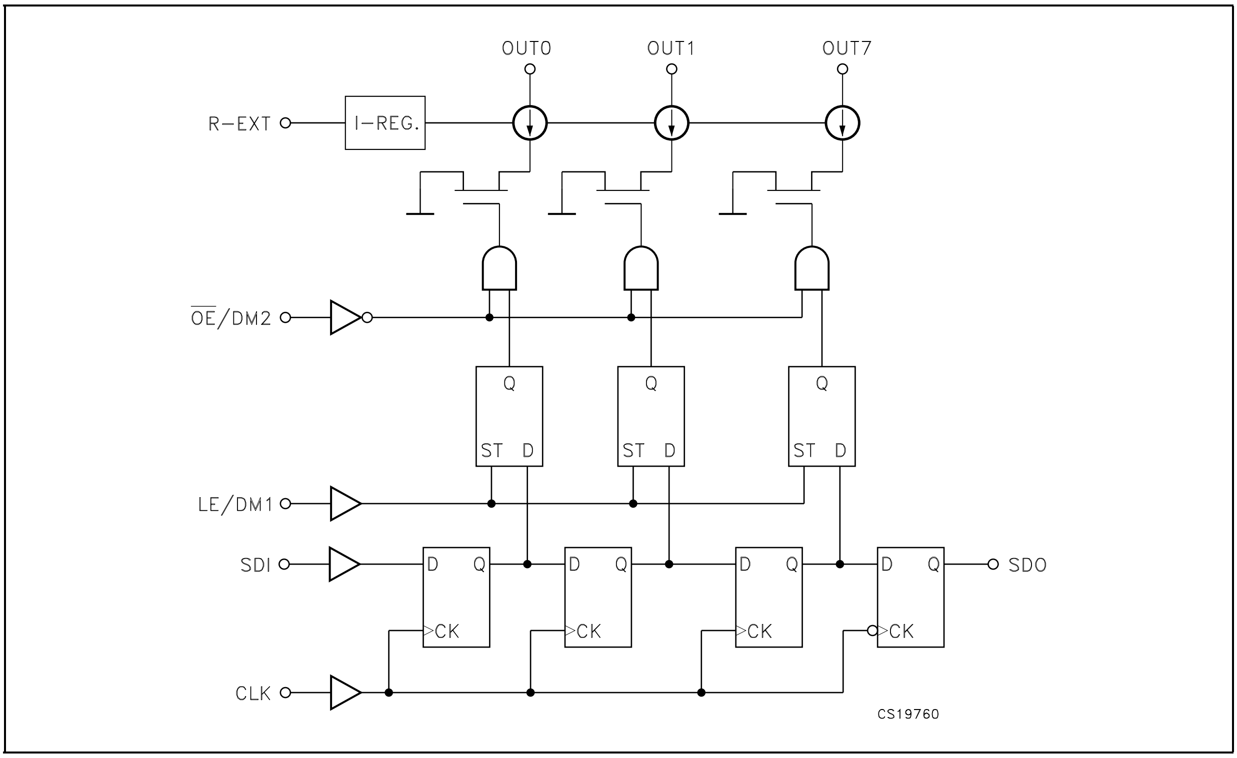
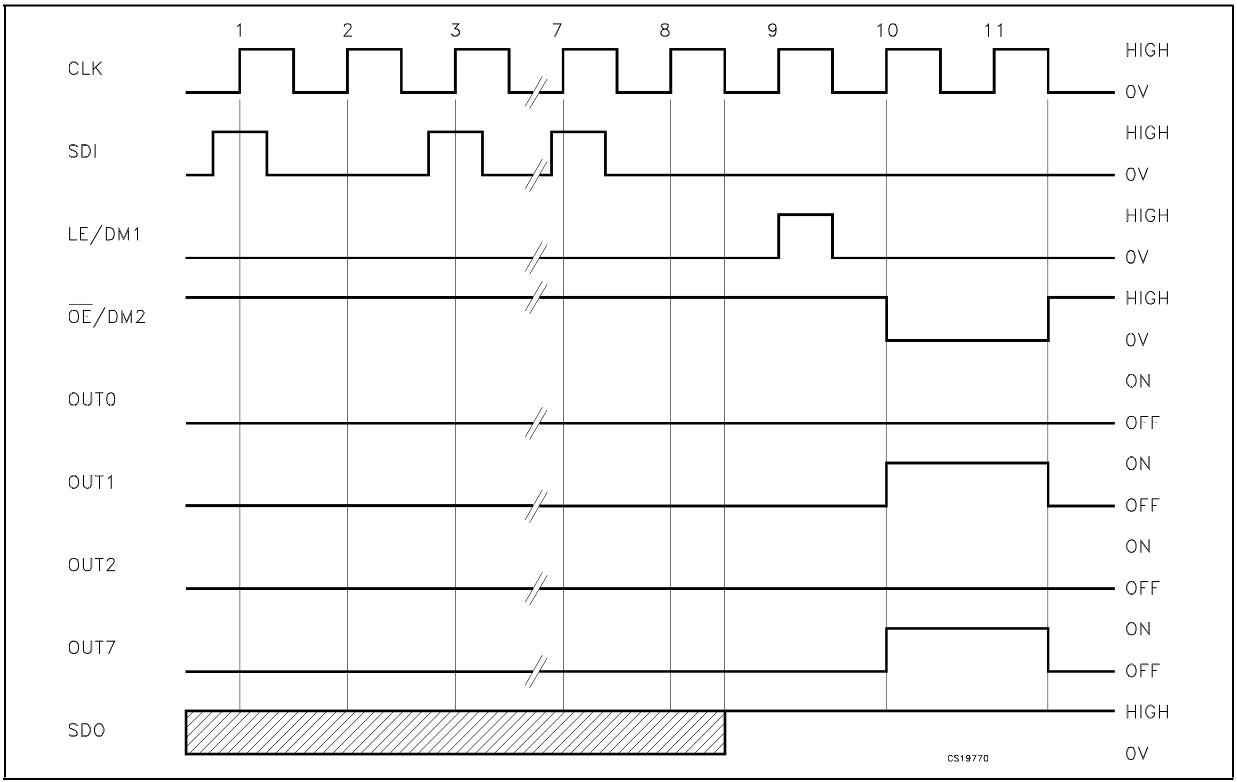
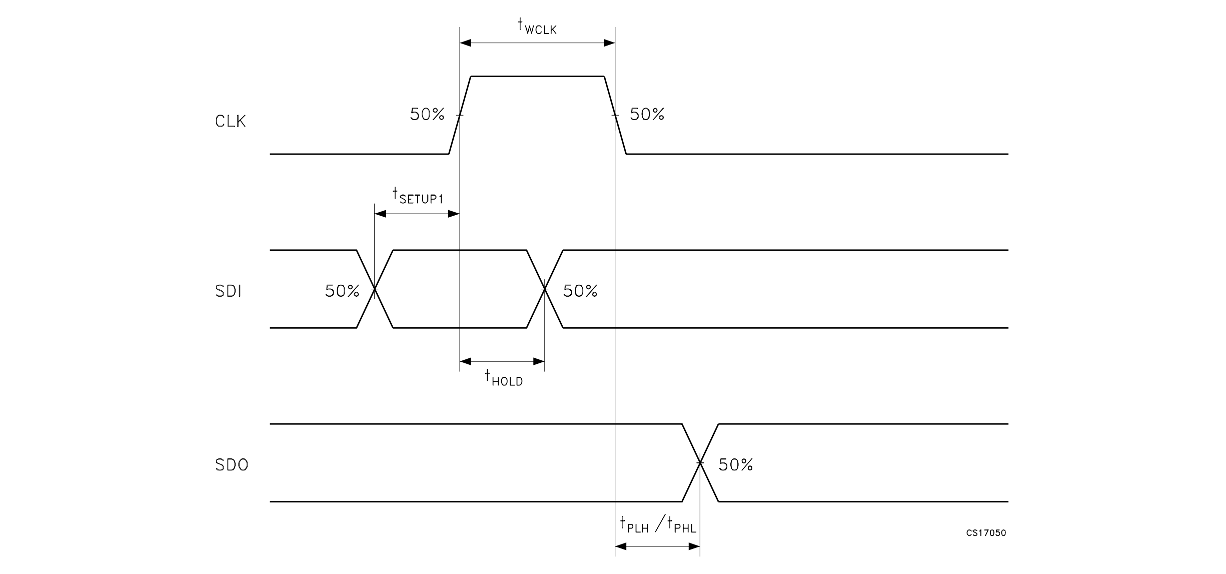



**Figure 7: Timing Diagram**




In normal mode the $\overline{OE}$/DM2 must remain low at least two clock cycles.

## Figure 8: Clock, Serial-In, Serial-Out




## Figure 9: Clock, Serial-In, Latch, Enable, Outputs

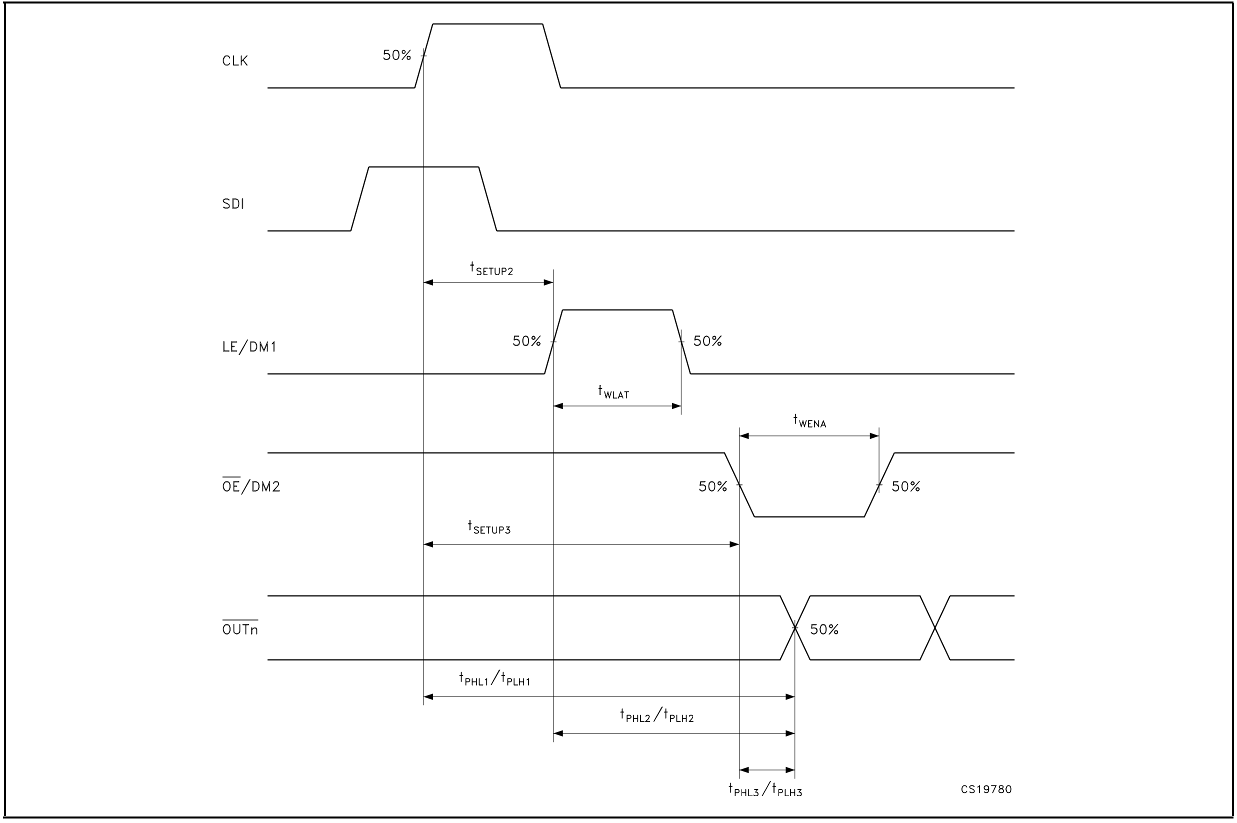
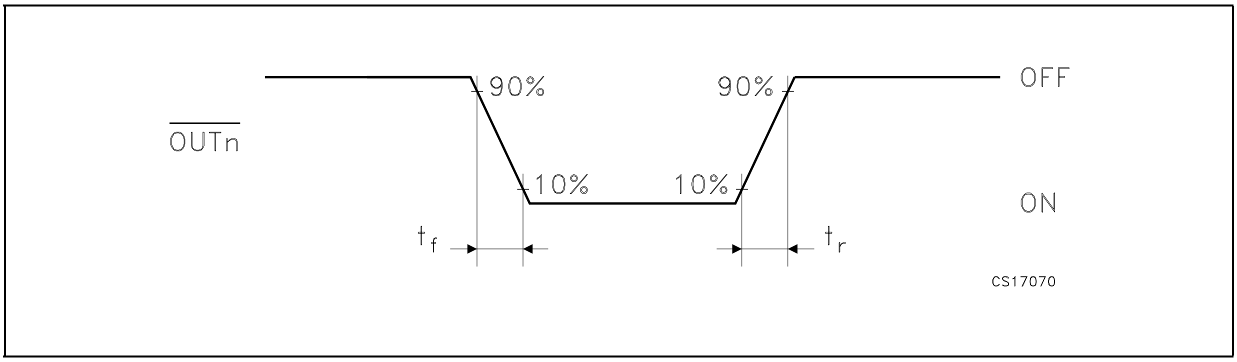


**Figure 10: Outputs**




## TEST CIRCUIT

**Figure 11: DC Characteristic**

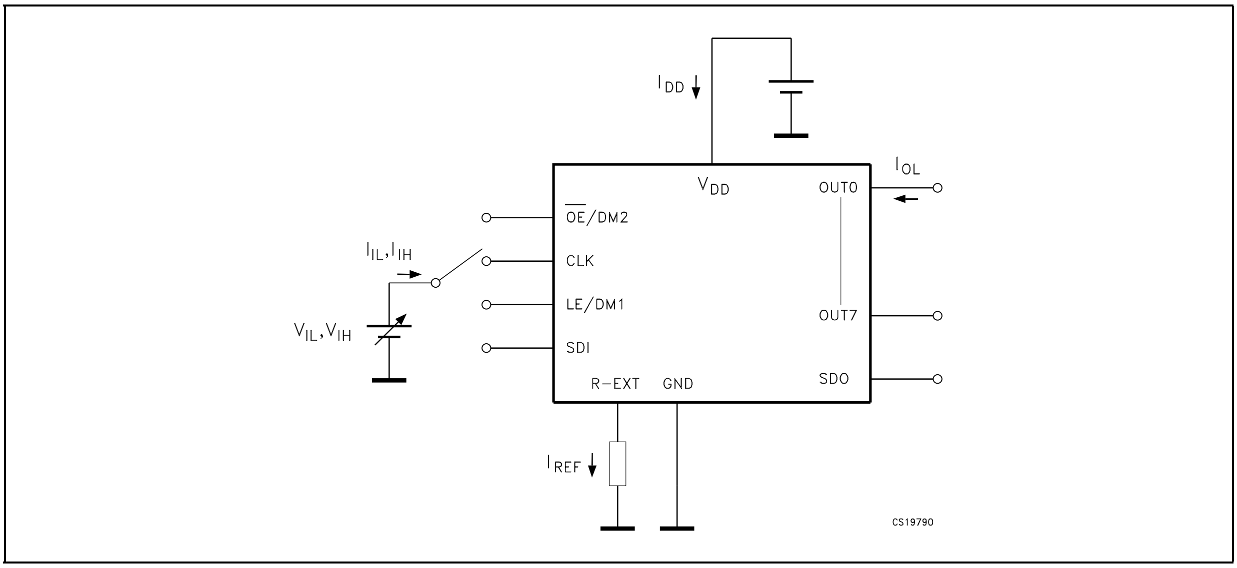
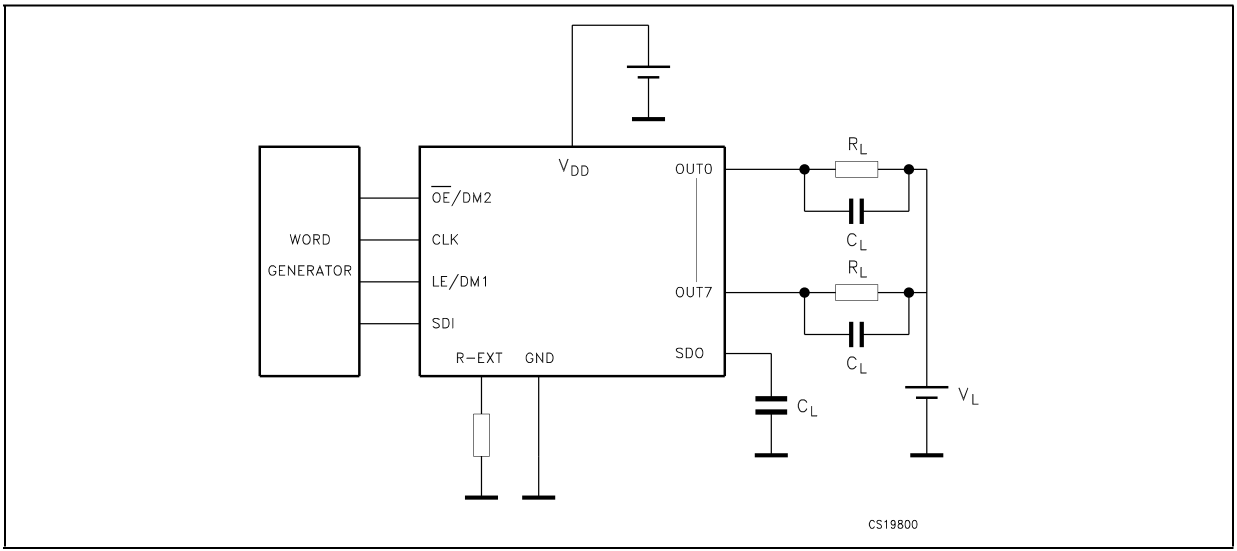



**Figure 12: AC Characteristic**



## RUNNING THE DETECTION MODE

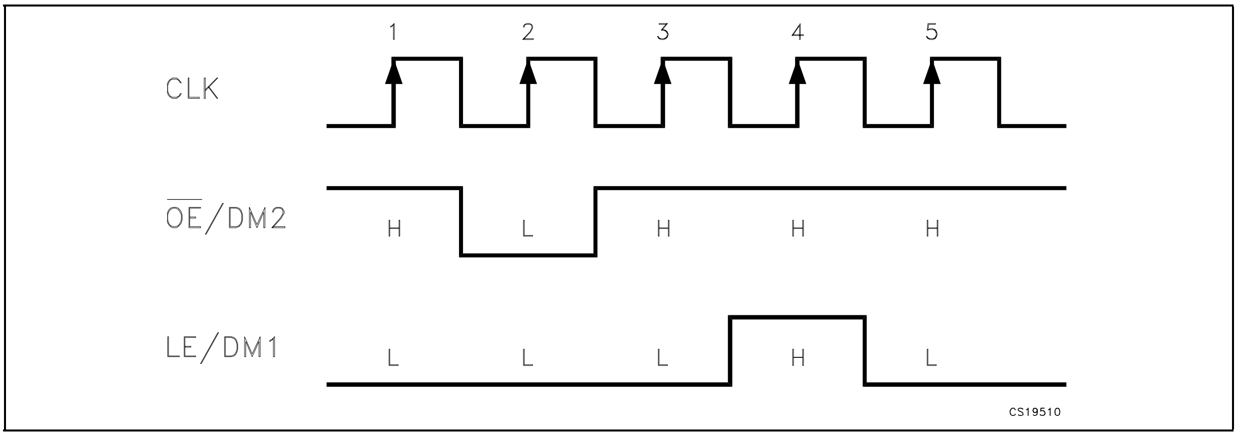
### Phase One: "Entering In Detection Mode"

From the "Normal Mode" condition the device can switch to the "Error Detection Mode" by a logic sequence on the OE/DM2 and LE/DM1 pins as showed in the following Table and Diagram:

**Table 9: Entering In Detection Truth Table**

| CLK | 1° | 2° | 3° | 4° | 5° |
|---|---|---|---|---|---|
| **OE/DM2** | H | L | H | H | H |
| **LE/DM1** | L | L | L | H | L |

**Figure 13: Entering In Detection Timing Diagram**

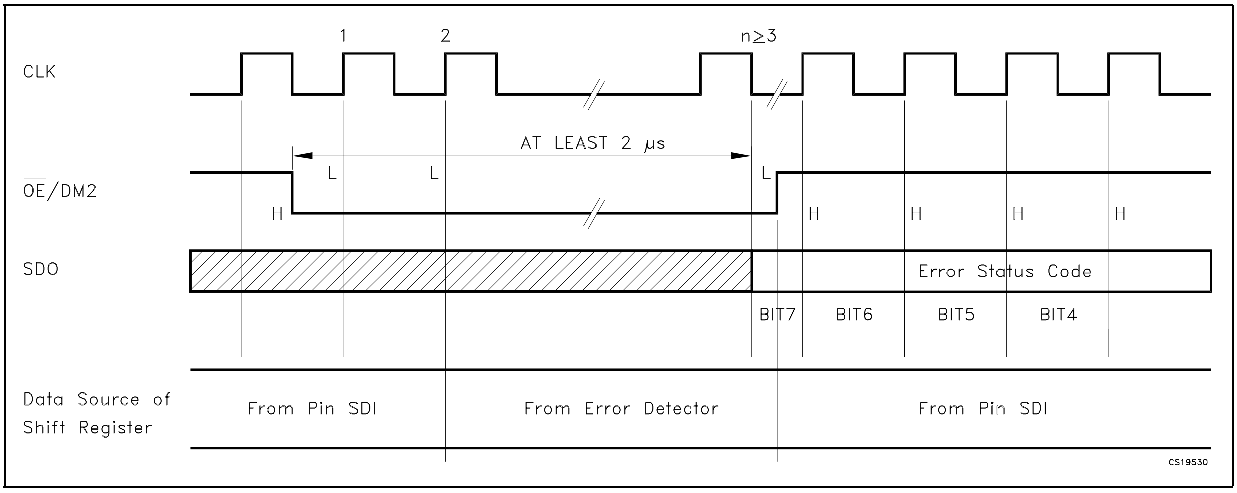



After these five CLK cycles the device goes into the" Error Detection Mode" and at the 6$^{th}$ rise front of CLK the SDI data are ready for the sampling.

### Phase Two: "Error Detection"

The eight data bits must be set "1" in order to set ON all the outputs during the detection. The data are latched by LE/DM1 and after that the outputs are ready for the detection process. When the Micro controller switches the OE/DM2 to LOW, the device drives the LEDs in order to analyze if an OPEN or SHORT condition has occurred.

**Figure 14: Detection Diagram**



The LEDs status will be detected al least in 2 microseconds and after this time the micro controller puts OE in HIGH state and the output data detection result will go to the microprocessor via SDO.

The detection data format is the same of data in normal mode. As soon as all the detection data bits are available on the serial line, the device may go back to normal mode operation.

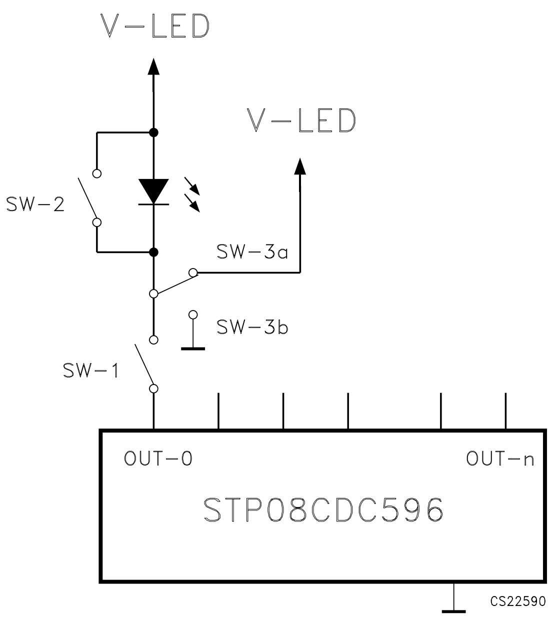
## CONDITIONS IN ORDER TO GET A SUCCESSFULLY DETECTION CONDITION

**Table 10: Detection Condition** ($V_{DD}$ = 3.3 to 5 V Temp. Range -40 to 85°C)

| | | | | |
|---|---|---|---|---|
| **SW-1 or SW-3b** | Open Line or Output Short to GND detected | ==> $I_{ODEC} \leq 0.5 \times I_O$ | No error detected | ==> $I_{ODEC} \geq 0.5 \times I_O$ |
| **SW-2 or SW-3a** | Short on LED or Short to V-LED detected | ==> $V_O \geq 2.4$ V | No error detected | ==> $V_O \leq 2.2$ V |

where: $I_O$ = the output current programmed by the $R_{EXT,}$ $I_{ODEC}$ = the detected output current in detection mode.

**Figure 15: Detection Mode**



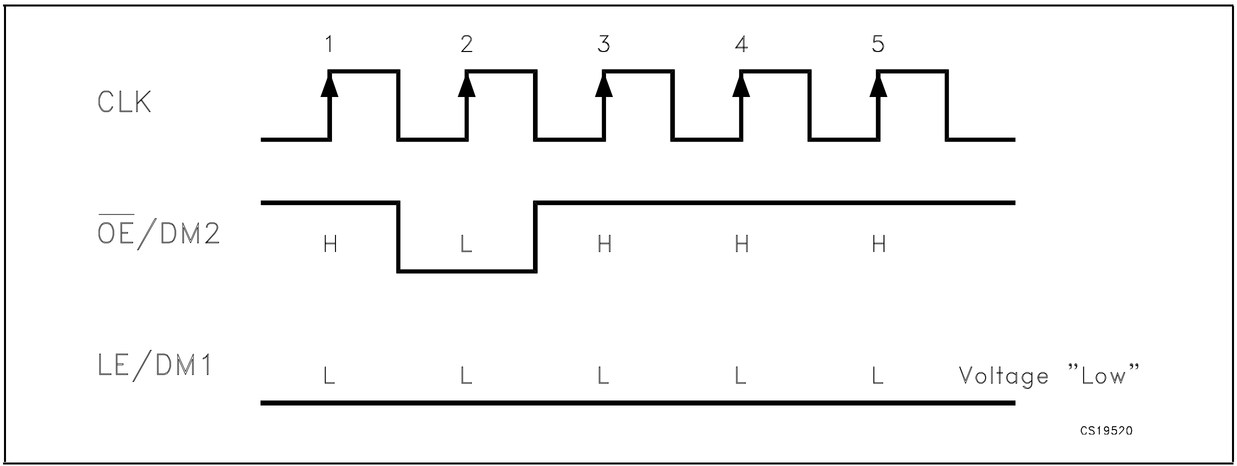
### Phase Three: “Resuming to Normal Mode”

The sequence for re-entering in normal mode is showed in the following Table and diagram:

**Table 11: Resuming to Normal Mode Timing Diagram**

| CLK | 1° | 2° | 3° | 4° | 5° |
|---|---|---|---|---|---|
| OE/DM2 | H | L | H | H | H |
| LE/DM1 | L | L | L | L | L |

**Figure 16: Resuming to Normal Mode Timing Diagram**




For proper device operation the "Entering in detection" sequence must be follow by a "Resume Mode" sequence, isn’t possible to insert consecutive equal sequence.

**Figure 17:** Typical Output Current-$R_{EXT}$ Resistor

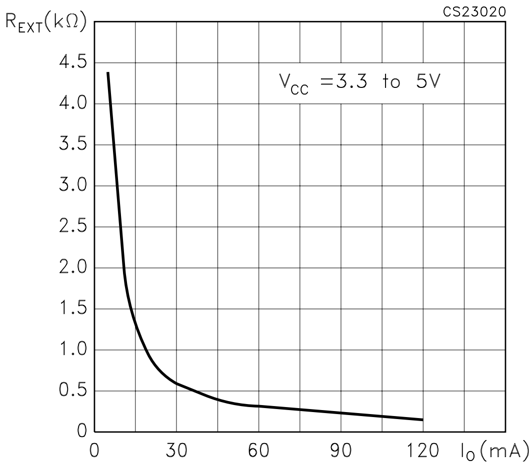



**Figure 18:** Power Dissipation vs Temperature Package

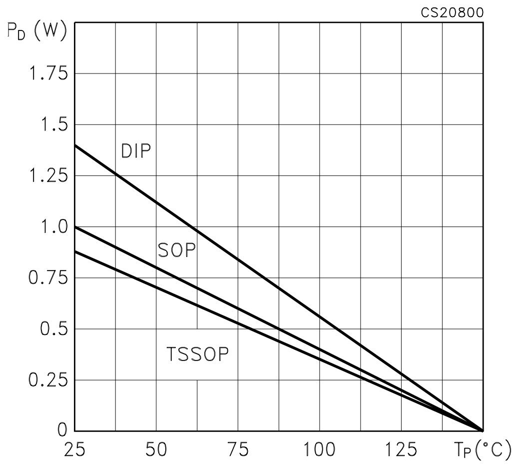



**Figure 19:** Typical Dropout Voltage vs Output Current

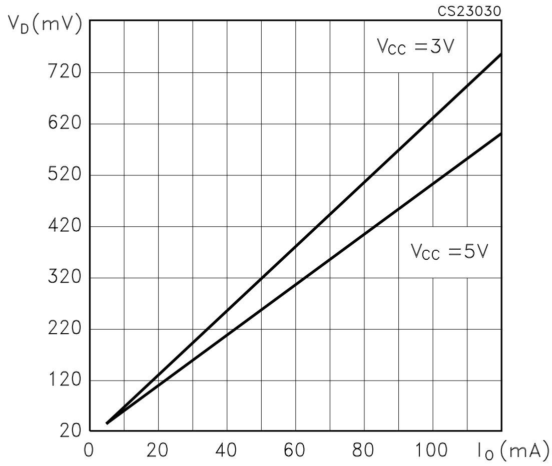



**Figure 20:** Typical Output Current vs $\pm\Delta I_{OL}$(%)

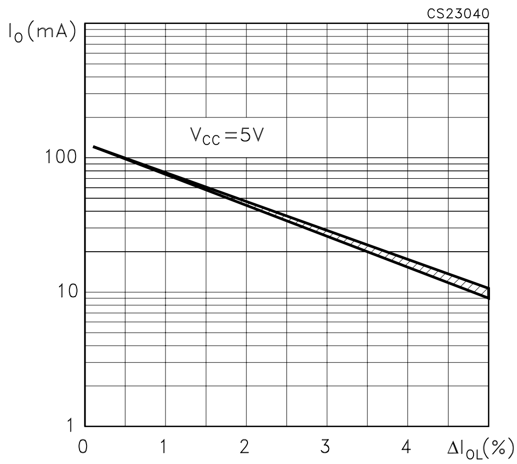
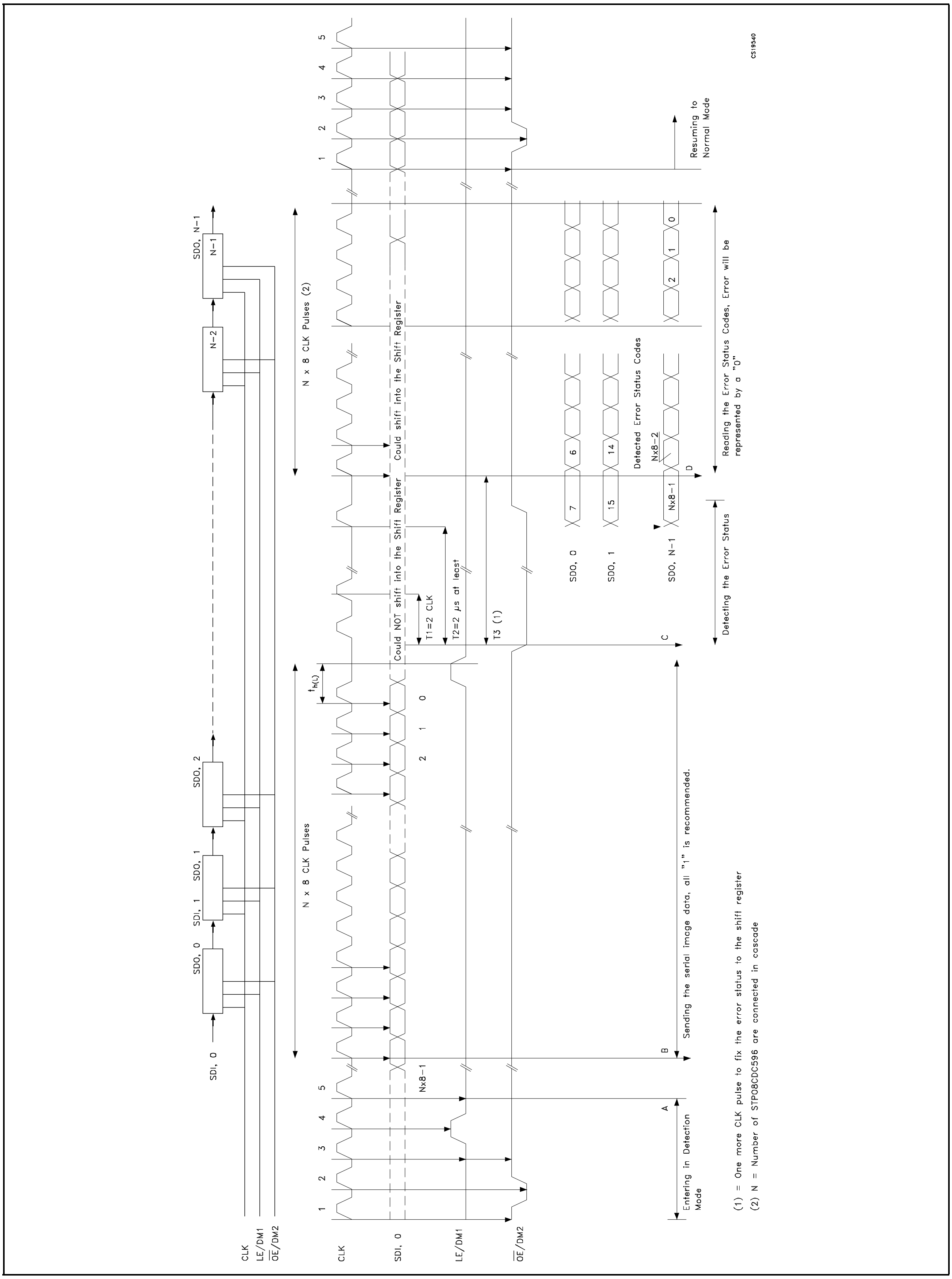
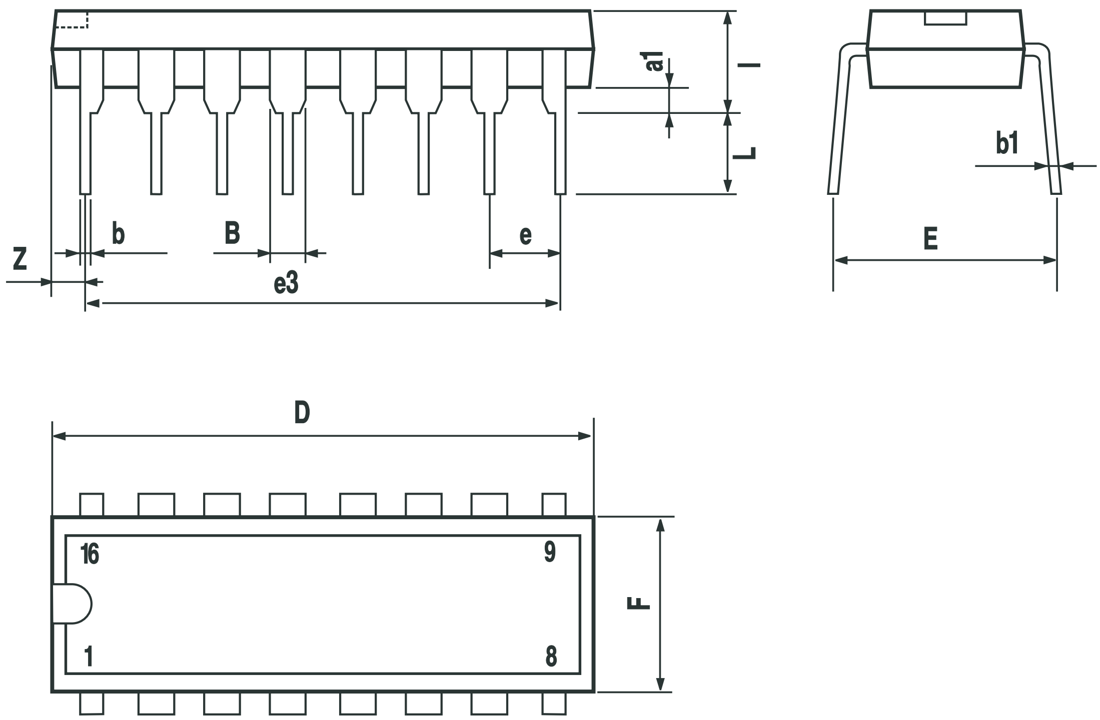


**Figure 21: Timing example for Open and/or Short detection**



## Plastic DIP-16 (0.25) MECHANICAL DATA

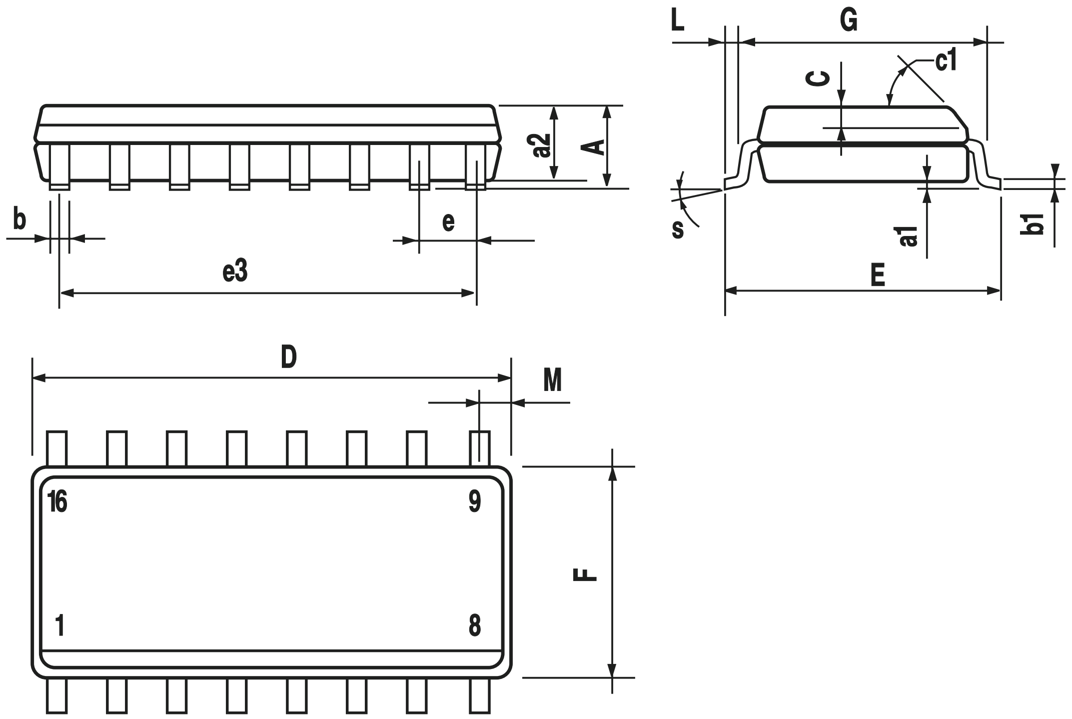
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |




P001C

## SO-16 MECHANICAL DATA

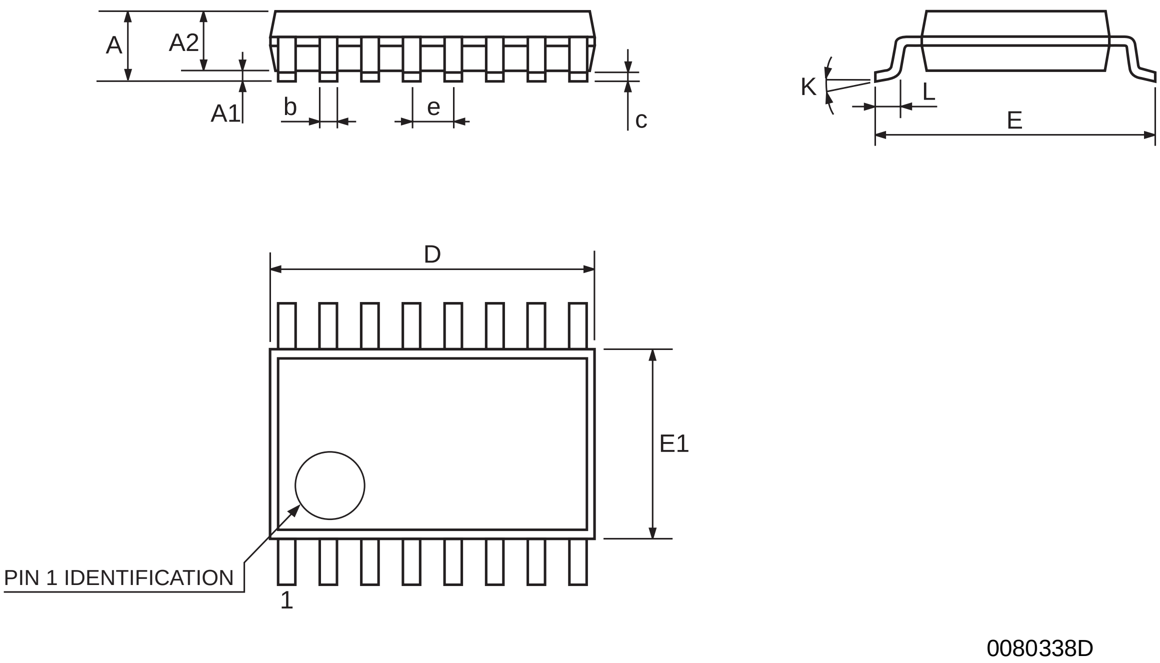
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.64 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8° (max.) | | | | | |




0016020D

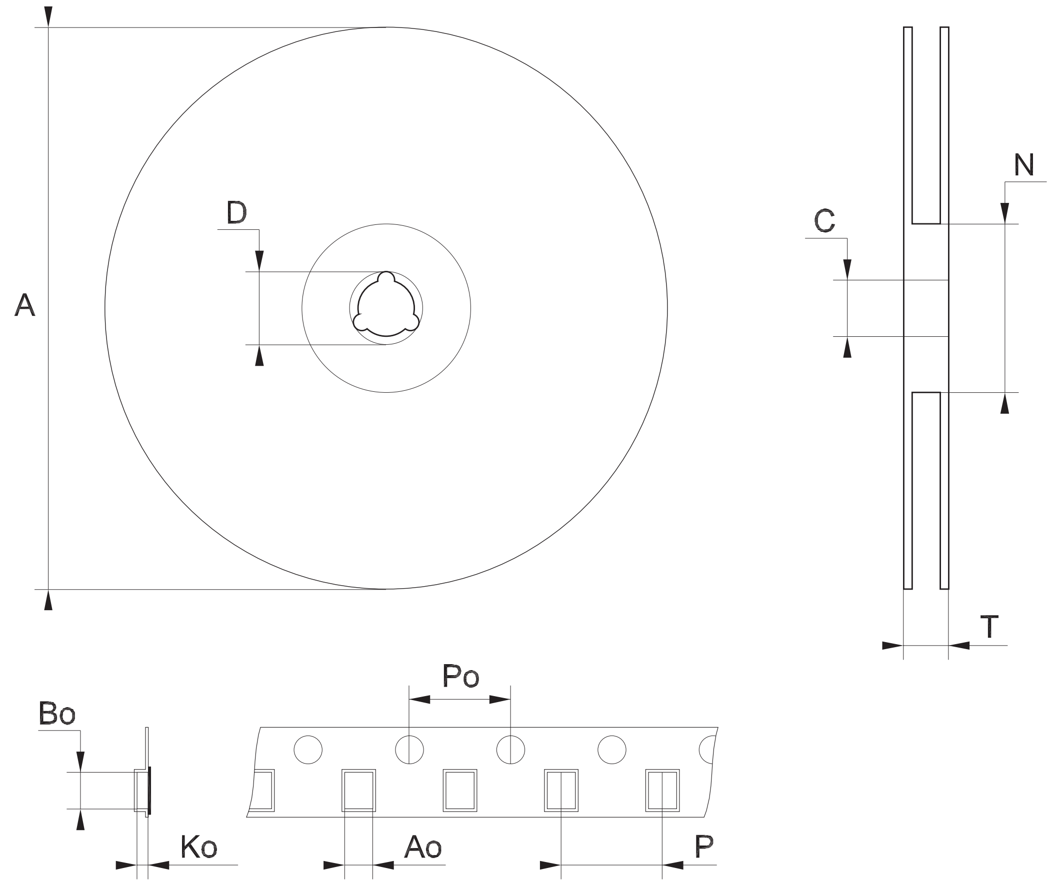
## TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.2 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.8 | 1 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | | 0.30 | 0.007 | | 0.012 |
| c | 0.09 | | 0.20 | 0.004 | | 0.0079 |
| D | 4.9 | 5 | 5.1 | 0.193 | 0.197 | 0.201 |
| E | 6.2 | 6.4 | 6.6 | 0.244 | 0.252 | 0.260 |
| E1 | 4.3 | 4.4 | 4.48 | 0.169 | 0.173 | 0.176 |
| e | | 0.65 BSC | | | 0.0256 BSC | |
| K | 0° | | 8° | 0° | | 8° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |



## Tape & Reel SO-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.45 | | 6.65 | 0.254 | | 0.262 |
| Bo | 10.3 | | 10.5 | 0.406 | | 0.414 |
| Ko | 2.1 | | 2.3 | 0.082 | | 0.090 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |




Note: Drawing not in scale

## Tape & Reel TSSOP16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 22.4 | | | 0.882 |
| Ao | 6.7 | | 6.9 | 0.264 | | 0.272 |
| Bo | 5.3 | | 5.5 | 0.209 | | 0.217 |
| Ko | 1.6 | | 1.8 | 0.063 | | 0.071 |
| Po | 3.9 | | 4.1 | 0.153 | | 0.161 |
| P | 7.9 | | 8.1 | 0.311 | | 0.319 |

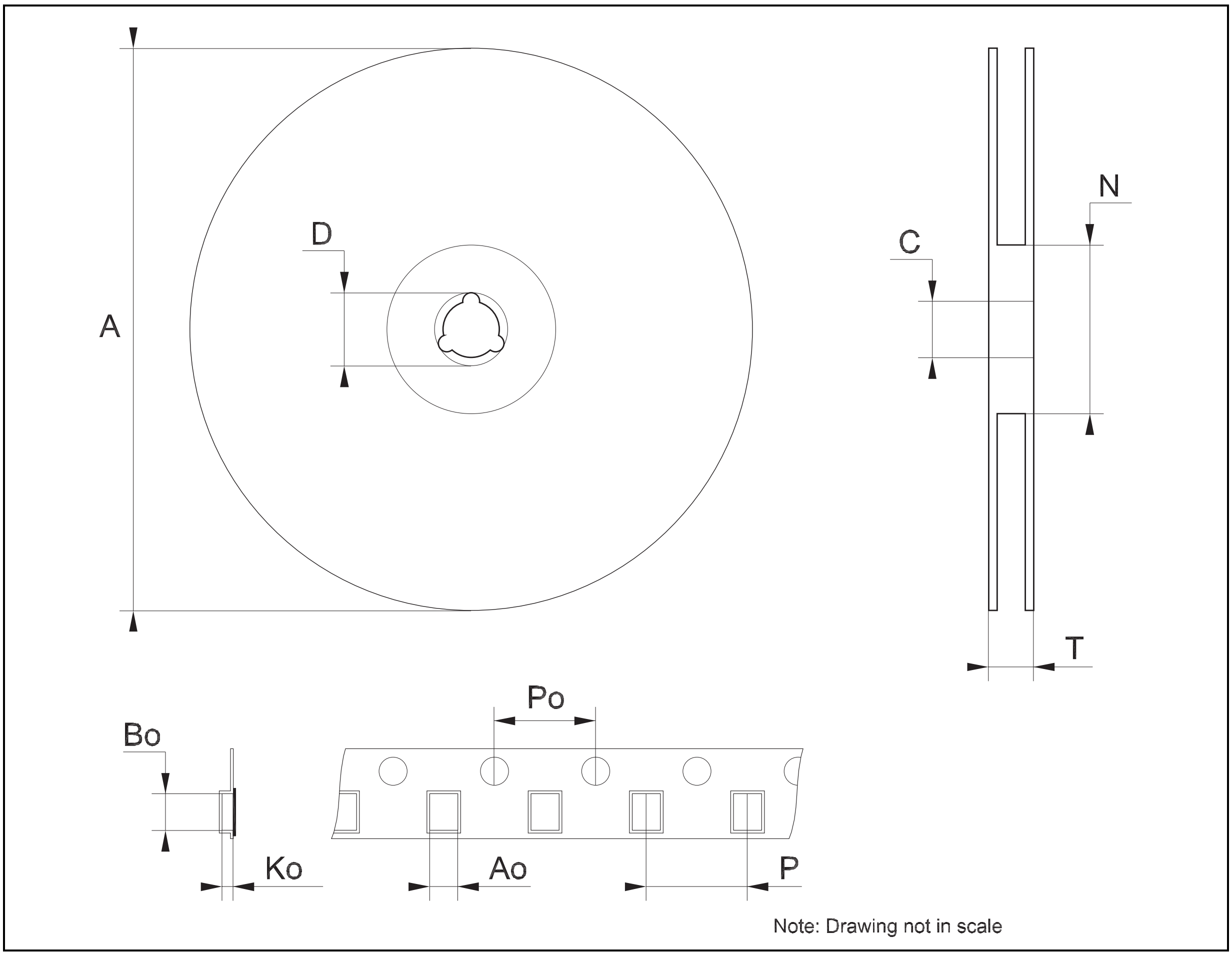


**Table 12: Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| 15-Jun-2005 | 1 | First Release. |
| 11-Oct-2005 | 2 | Minor Revision |